## REMARKS

With this Response, Applicants respectfully request that claim 20 be canceled without prejudice. Furthermore, Applicants have amended claims 1 and 19. Therefore, claims 1-11, 19, 21-24, and 29-35 are pending.

## ALLOWABLE SUBJECT MATTER

Applicants acknowledge that claims 29-35 have been allowed.

Applicants acknowledge that claims 3 and 11 were found to have allowable subject matter. Specifically, these claims were objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants respectfully submit that the rejection of the independent claims is overcome herein, rendering these allowable as written.

Additionally, Applicants acknowledge that claim 24 was found to have allowable subject matter. Specifically, this claim was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, second paragraph, set forth in the present Office Action and to include all of the limitations of the base claim and any intervening claims. Applicants respectfully submit that the issues under 35 U.S.C. § 112, second paragraph, as well as the substantive rejections of the independent claim are overcome herein, rendering this claim allowable as written.

## CLAIM REJECTIONS - 35 U.S.C. § 112

Claims 6 and 19-24 were rejected under 35 U.S.C. § 112, second paragraph, as being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Specifically, these claims were rejected as failing to define the expression "high-resistivity silicon" as used in these claims.

Regarding claim 6, Applicants submit that "high-resistivity silicon" would be understood by the skilled practitioner as silicon that is undoped, but is rather statistically "pure," as referring to the highest practical purities obtainable from known techniques for producing silicon wafers. Such silicon is generally about 100 Ω-cm or higher, as contrasted to lightly doped silicon used in general CMOS processing, which is orders of magnitude more conductive (on the order of single Ω-cm). Thus, claim 6 refers to undoped silicon used for the substrate.

Regarding claims 19-24, Applicants amend claim 19 herein to remove reference to "high-resistivity" silicon. Thus, claim 19 as amended renders the rejection moot. The only reference within the set of claims 19-24 was found in independent claim 19. Thus, Applicants respectfully submit that removing reference to such a limitation in the independent claim renders moot the rejection as applied to claims 21-24 (claim 20 is canceled herein, rendering rejection of this claim moot).

## CLAIM REJECTIONS - 35 U.S.C. § 103

### Rejections Under Lin

Claims 1, 6, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 4,672,421 of Lin (hereinafter "Lin"). Applicants respectfully submit that these claims are not rendered obvious by the cited reference for at least the following reasons.

Claim 1 as amended herein recites the following:

> a silicon substrate;
> contact pads processed on the silicon substrate to connect to an integrated circuit (IC) die;
> interconnections selectively interconnecting the contact pads, the interconnections monolithically processed on the silicon substrate; and
> **circuit elements monolithically processed on the silicon substrate in the same plane as the interconnections** with the same processing as the contact pads and the interconnections, the circuit elements to interoperate with the IC die.

Claims 6, 8, and 9 depend from claim 1, and therefore necessarily include the limitations of claim 1.

As Applicants have understood Lin, the reference discusses mounting ICs on a substrate. Specifically, the ICs can be bonded to other ICs or to "external" circuit elements, which Applicants have understood to be circuit elements external to the ICs. See col. 4, lines 4 to 18 and col. 5, lines 3 to 8. Applicants do not understand the external circuit elements to be elements that are monolithically processed on the silicon substrate in the same plane as interconnections, as recited in claim 1. Therefore, Applicants submit that claim 1 includes at least one feature not disclosed or suggested by the cited reference, and is thus patentable over the cited reference.

### Rejections Under Shrauger

Claims 1, 2, 4-9 and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent Publication No. 2003/0020094 of Shrauger (hereinafter "Shrauger"). Claim 20 is

canceled herein, rendering rejection of this claim moot. Applicants submit that the remaining claims are not rendered unpatentable by the cited reference for at least the following reasons.

Claim 1 is set forth above. Claim 19 similarly refers to functional circuit elements monolithically embedded in a silicon substrate in the same plane as interconnect elements of the silicon substrate. Thus, Applicants respectfully submit that the arguments with respect to claim 1 should apply equally well to claim 19 with regard to arguments focusing on circuit elements monolithically processed in a silicon substrate in the same plane as interconnection elements. Specifically in the Office Action at page 5, MEMS die M is referenced as disclosing the claimed circuit elements. Applicants respectfully submit that MEMS die M is a separate IC, bonded to the interconnect backplane as are other ICs. Thus, the MEMS die cannot disclose a circuit element monolithically processed in a silicon substrate in the same plane as the interconnection elements, in contrast to what is claimed. Thus, Applicants respectfully submit that the Shrauger reference fails to disclose or suggest at least one element of the invention as recited in Applicants' independent claims. The dependent claims necessarily include the limitations of the independent claims from which they depend; therefore, the references likewise fail to disclose at least one feature of the dependent claims.

**Rejections Under Baugh**

Claims 1, 5-10, 19, 21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,998,691 of Baugh et al. (hereinafter "Baugh"). Applicants submit that these claims are not rendered unpatentable by the reference for at least the following reasons.

Both claims 1 and 19 are independent claims, and both make reference to circuit elements monolithically processed in a silicon substrate in the same plane as interconnection elements. The Baugh reference fails to disclose or suggest such features as claimed. Consider Figure 3A of the reference, which discloses a layered process for providing connection elements and connection points. Consider also US Patent Application Publication No. 2005/0063431 (submitted in an Information Disclosure Statement concurrently herewith), which is a copending application with Baugh, and is incorporated by reference into Baugh. 2005/0063431 similarly discusses layered semiconductor devices, and embodies the process referred to at col. 5, lines 50 to 55 by which Figure 3A may be made. As Applicants have understood, the reference fails to disclose or suggest circuit elements monolithically processed in a silicon substrate in the same

plane as interconnection elements. Thus, Applicants respectfully submit that the cited reference fails to disclose or suggest at least one feature of the invention as recited in the independent claims. The dependent claims necessarily include all limitations of the independent claims from which they depend; therefore, the references likewise fail to disclose at least one feature recited in the dependent claims.

**Rejections Under Reference Combination**

Claim 22 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Baugh in view of US Patent No. 6,420,197 of Ishida et al. (hereinafter "Ishida"). Claim 22 depends from claim 19, which is discussed above with respect to the Baugh reference. The Ishida reference is not cited as curing the deficiencies of the Baugh reference pointed out above. Rather Ishida is cited as disclosing that an IC with a silicon substrate is bonded to another silicon substrate. Whether or not the reference discloses what is asserted, Applicants do not understand Ishida to cure the deficiencies of Baugh. Whether alone or in combination, the references fail to disclose or suggest at least the feature of independent claim 19 of circuit elements monolithically processed in a silicon substrate in the same plane as interconnection elements. Thus, Applicants respectfully submit that the references, whether alone or in combination, fail to render obvious the invention as recited in claim 22, which depends from claim 19 and necessarily includes all the limitations of claim 19.

**CONCLUSION**

For at least the foregoing reasons, Applicants submit that the rejections of the claims have been overcome herein, placing all pending claims in condition for allowance. Applicants respectfully request that the rejections of the claims be withdrawn, and the claims be allowed. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the above-referenced application.

The Commissioner is hereby authorized to charge or credit any deficiencies or over-payments to Deposit Account No. 02-2666.

Respectfully submitted,

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